Power over Ethernet Consortium
Clause # 33 PSE Conformance Test Suite v 2.2 Report

UNH-IOL — 121 Technology Drive, Suite 2 — Durham, NH 03824 — +1-603- 862-4196
Consortium Manager: Gerard Nadeau — grn@iol.unh.edu — +1-603- 862-0166

David Rakovsky
GlobTek, Inc.
186 Veterans Dr.
Northvale, NJ 07647

September 11, 2006
Report Rev. 1.0

Enclosed are the results from the Clause # 33 PSE Conformance testing performed on:

Device Under Test (DUT):	GlobTek GT-91085-1548
Port Tested:	Output
Hardware Version:	Not Available
DUT PHY Chip:	Not Applicable
Power Chipset:	Not Available

The test suite referenced in this report is available at the UNH-IOL website:

ftp://ftp.iol.unh.edu/pub/ethernet/test_suites/CL33_PSE/PSE_Test_Suite_v2.0.pdf

Issues Observed While Testing
33.3.1 – Overload Current Detection Range – The overload current was above the maximum conformant value.
33.3.3 – Inrush Current - The peak inrush current, measured after 1ms, was above the maximum conformant value. The mode inrush current value was below the minimum conformant value.
33.4.1 – Midspan PSE Return Loss – The return loss was observed to be below the conformance limit.
33.4.2 – Midspan PSE Insertion Loss – The insertion loss was observed to be above the conformance limit.

For specific details regarding issues please see the corresponding test result.

Testing Completed 08/09/2006

David Schwarzenberg
dws2@iol.unh.edu

Digitally signed by UNH-IOL
Date: 2006.09.11 12:38:23 -04'00'

Review Completed 09/11/2006

Zachary Clifton
zclifton@iol.unh.edu

Digital Signature Information

This document was created using an Adobe digital signature. A digital signature helps to ensure the authenticity of the document, but only in this digital format. For information on how to verify this document's integrity proceed to the following site:

http://www.iol.unh.edu/certifyDoc

If the document status still indicates "Validity of author NOT confirmed", then please contact the UNH-IOL to confirm the document's authenticity. To further validate the certificate integrity, Adobe 6.0 should report the following fingerprint information:

MD5 Fingerprint: A569 F807 031D B1EC E509 4110 95E3 5362
SHA-1 Fingerprint: F007 7D91 2FAA A22C A3D9 F93F 05AC 09DB E219 84B2

Result Key

The following table contains possible results and their meanings:

Result	Interpretation
PASS	The Device Under Test (DUT) was observed to exhibit conformant behavior.
PASS with Comments	The DUT was observed to exhibit conformant behavior however an additional explanation of the situation is included, such as due to time limitations only a portion of the testing was performed.
FAIL	The DUT was observed to exhibit non-conformant behavior.
Warning	The DUT was observed to exhibit behavior that is not recommended.
Informative	Results are for informative purposes only and are not judged on a pass of fail basis.
Refer to Comments	From the observations, a valid pass or fail could not be determined. An additional explanation of the situation is included.
Not Applicable	The DUT does not support the technology required to perform these tests.
Not Available	Due to testing station or time limitations, the tests could not be performed.
Borderline	The observed values of the specified parameters are valid at one extreme, and invalid at the other.
Not Tested	Not tested due to the time constraints of the test period.

Test Setup

Testing Equipment	
Real-time DSO	TEKTRONIX, TDS 3014
Current Probe and Amplifier	TEKTRONIX, TPS305 and TPSA300
Digital Multimeter	HEWLETT-PACKARD, 34401A
Digital Power Supply	AGILENT TECHNOLOGIES, E3641A
Arbitrary Waveform Generator	SONY/TEK,AWG2041,0,CF:91.1CT FV:1.26
Vector Network Analyzer	"HEWLETT-PACKARD,8712B,US34400165,B.03.02"
UNH-IOL Developed Test Board	PoE Test Board Version 1.0

Basic Testing Configuration

The basic testing configuration is defined in the UNH Interoperability Laboratory PSE Parametric Test Suite v2.2

GROUP 1: DETECTION CHARACTERISTICS

Test # and Label	Part(s)	Result(s)
33.1.1 – PSE location	**a**	**PASS**
Expected Results and Procedural Comments		
Purpose: To verify that the PSE is in a valid location with respect to the link segment, and it performs detection and powers on the correct set of pins. a. A PSE operating as an endpoint must perform detection and apply power on Alternative A or Alternative B. A PSE operating as a midspan must perform detection and supply power on the Alternative B pairs. An Alternative B device must supply positive Vport on pins 4 and 5, and negative Vport on pins 7 and 8.		
Comments on Test Results		
a. The PSE is in a valid location and powers on the correct set of pins.		

Test # and Label	Part(s)	Result(s)
33.1.2 - Detection Circuit	**a**	**PASS**
Expected Results and Procedural Comments		
Purpose: To verify the Thevenin equivalent detection circuit of the PSE detection source. a. The DUT loaded circuit voltage should be less than half the open circuit PI voltage or reject current into $V_{detect+}$. The open circuit voltage should not exceed 30V.		
Comments on Test Results		
a. Open circuit voltage = 8.5 V The DUT was observed to reject current into Vdetect+ port. This is compliant with the Alternative PSE detection source shown in Figure 33-9. Output Impedance was not calculated (not applicable due to diode configuration).		

Test # and Label	Part(s)	Result(s)
33.1.3 - BackDrive Current	**a**	**PASS**
Expected Results and Procedural Comments		
Purpose: To verify that the detection circuit of the PSE can withstand maximum backdrive current over the range of V_{Port}. a. The DUT should not be affected by backdrive current		
Comments on Test Results		
a. The DUT was observed to properly ignore the backdrive current.		

Test # and Label	Part(s)	Result(s)
33.1.4 - Open Circuit Voltage	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the open circuit voltage at the PI of the PSE during detection mode is below the conformance limits.

b. The open circuit voltage (V_{oc}) should not exceed 30 Volts.

Comments on Test Results

b. Open Circuit Voltage = 8.5 V

Test # and Label	Part(s)	Result(s)
33.1.5 – Detector Circuit Output Current	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the short circuit output current of the PSE during PD detection is within the conformance limits.

a. The output short circuit current should not exceed 5 mA.

Comments on Test Results

a. The observed short circuit output current was 0.9 mA.

Test # and Label	Part(s)	Result(s)
33.1.6 – Detector Circuit Output Voltage	**a**	**PASS**
	b	**PASS**
	c	**PASS**

Expected Results and Procedural Comments

Purpose: To verify the voltage output of the PSE's detection circuit conforms to the specified limits.

a. The loaded circuit voltage should be between 2.8 and 10V.
b. The voltage difference between any consecutive detection probe voltages should be at least 1V.
c. The slew rate of the probe voltages should be no greater than 0.1V/µs.

Comments on Test Results

a. Probe Voltage1 = 4.02 V
   Probe Voltage2 = 8.09 V
b. Detection probe voltage difference = 4.07 V
c. Maximum slew rate of the probe voltages = 0.07 V/µs

Please refer to the figures appended to the report.

Test # and Label	Part(s)	Result(s)
33.1.7 – PD Detection Timing	**a**	**PASS**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the PSE probes its PI with valid detection pulses and completes an entire detection sequence within the proper time period.

a. The total pulse width of the detection pulse should not be greater than 500ms.
b. The detection probe voltages should have a duration of at least 2 ms.

Comments on Test Results

a. Probe Voltage1 pulse width = 90.4 ms
   Probe Voltage2 pulse width = 90.3 ms
b. Duration of the detection probe voltages > 2 ms

Please refer to the figures appended to the report.

Test # and Label	Part(s)	Result(s)
33.1.8 – PD Signature Detection Limits	**a**	**PASS**
	b	**PASS**
	c	**PASS**
	d	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT will properly detect a PD's Signature impedance.

a. The minimum accepted input resistance should be between 15 kΩ and 19 kΩ.
b. The maximum accepted input resistance should be between 26.5kΩ and 33 kΩ.
c. The DUT must detect a proper signature if the input capacitance is less than 150nF.
d. The DUT must accept capacitances below 10µF and reject capacitances above 10µF.

Comments on Test Results

a. 16.7 kΩ ≤ $R_{accept(min)}$ ≤ 16.8 kΩ
b. 29.8 k Ω ≤ $R_{accept(max)}$ ≤ 29.9 kΩ
c. The DUT was observed to accept capacitances less than 150nF.
d. The DUT was observed to reject improper capacitances above 10µF.

Test # and Label	Part(s)	Result(s)
33.1.9 – PD Classification	**a**	**Not Applicable**
	b	**Not Applicable**
	c	**Not Applicable**
	d	**Not Applicable**

Expected Results and Procedural Comments

Purpose: To verify that a DUT supporting Classification properly performs PD class detection.

a. During classification the PSE should supply a voltage between 15.5 and 20.5 V.
b. The DUT should accurately classify the PD.
c. The DUT should classify the PD as Class 0 if the current drawn is equal to or greater than 51mA.
d. The DUT should not supply a current greater than 100 mA.

Comments on Test Results

The DUT does not implement classification.

Test # and Label	Part(s)	Result(s)
33.1.10 – Classification Timing	**a**	**Not Applicable**

Expected Results and Procedural Comments

Purpose: To verify that a PSE capable of classifying a PD completes classification within the proper time period after successfully completing the detection of a PD.

a. The DUT should complete classification between 10ms and 75ms after PD detection.

Comments on Test Results

The DUT does not implement classification.

Test # and Label	Part(s)	Result(s)
33.1.11 – New Detection Cycle	**a**	**PASS**
Expected Results and Procedural Comments		
Purpose: To verify that if the PSE is unable to supply power within T_{pon} then, it initiates and successfully completes a new detection cycle before powering on. a. The DUT should complete a full detection cycle before applying power onto the link segment.		
Comments on Test Results		
a. The DUT was observed to successfully complete a new detection cycle before applying power onto the link segment.		

Test # and Label	Part(s)	Result(s)
33.1.12 – Alternative A Backoff Cycle	**a**	**Not Applicable**
Expected Results and Procedural Comments		
Purpose: To verify that if a PSE implementing Alternative A detects an invalid signature at its PI, it will resume detection within the maximum conformant time. a. The DUT should resume detection in times less than 1 seconds.		
Comments on Test Results		
The DUT was configured for alternative B, see test #33.1.13.		

Test # and Label	Part(s)	Result(s)
33.1.13 – Alternative B Backoff Cycle	**a**	**PASS**
	b	**PASS**
Expected Results and Procedural Comments		
Purpose: To verify that if a PSE implementing Alternative B fails to detect a valid detection signature at its PI, it will wait for the appropriate period of time before beginning a new detection cycle and applies a voltage on to the PI that falls within the defined limits. a. The DUT should not apply a voltage greater than 2.8 V_{dc} to the PI. b. The value for T_{dbo} should be at least 2 sec.		
Comments on Test Results		
a. The DUT was observed to not apply a voltage greater than 2.8 V_{dc} to the PI. a. The DUT was observed to wait for 2.9 seconds before resuming detection.		

GROUP 2: POWER FEED CHARACTERISTICS

Test # and Label	Part(s)	Result(s)
33.2.1 – Turn On Rise Time	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that when the PSE turns on power, the response times of the PSE are within the conformance limits.

a. The measured slew rate should not exceed 3.04V/µs.

Comments on Test Results

a. The observed slew rate was 0.04 V/µs

Please refer to the figures appended to the report.

Test # and Label	Part(s)	Result(s)
33.2.2 – Power Feed Ripple and Noise	**a**	**Informative**
	b	**Informative**
	c	**Informative**
	d	**Informative**

Expected Results and Procedural Comments

Purpose: To verify that the power feeding ripple and noise are within the conformance limits.

The peak-to-peak values of ripple and noise transmitted on the line by the DUT, in both the common mode and pair-to-pair, should not exceed:
a. 0.5 V_{pp} between 0-500 Hz
b. 0.2 V_{pp} between 500 Hz -150 kHz
c. 0.15 V_{pp} between 150-500 kHz
d. 0.1 V_{pp} between 500 kHz-1 MHz

Comments on Test Results

Total Ripple and Noise = 0.05 V_{pp}

Note: This test is currently under development. Individual frequency range information is not currently available.

Test # and Label	Part(s)	Result(s)
33.2.3 – Load Regulation	**a**	**Not Available**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the PSE performs load regulation while supplying power to the PI.

a. Voltage transients should not exceed 3.5 V/µs.
b. The DUT output voltage should be between 44 and 57 V for all values of I_{Port}.

Comments on Test Results

a. This test is currently under development.
b. V_{Port} (max)= 48.9 V
   V_{Port} (min)= 48.2 V

Test # and Label	Part(s)	Result(s)
33.2.4 – Power Turn On Timing	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT supplies power onto the link segment within the acceptable turn on time after it has successfully detected a PD.

a. The DUT should start supplying power within T_{pon} (400ms) after detection.

Comments on Test Results

a. The DUT was observed to supply power immediately (less than 1ms) after detection.

Test # and Label	Part(s)	Result(s)
33.2.5 – Apply Power	**a**	**PASS**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the PSE applies power on the same pairs as those used for detection after completing a valid detection.

a. The PSE should perform a valid detection sequence before powering the PD.
b. The PSE should supply power on the same pairs as that it performed detection for the PD.

Comments on Test Results

a. The DUT performed a valid detection sequence before supplying power onto the link segment.
b. The DUT applied power on the same pairs as those it detected on.

Test # and Label	Part(s)	Result(s)
33.2.6 – PSE Current Unbalance	**a**	**PASS**
Expected Results and Procedural Comments		
Purpose: To verify that the current unbalance between the two conductors of the power pairs of the PSE over the current load range is within the permissible range. a. The current unbalance between the two conductors per power pair should not be greater than 10.5mA.		
Comments on Test Results		
a. The DUT was observed to have a current unbalance less than 3.0 mA for minimum and maximum I_{port}.		

GROUP 3: ERROR DETECTION AND POWER REMOVAL

Test # and Label	Part(s)	Result(s)
33.3.1 – Overload Current Detection Range	**a**	**FAIL**
	b	**PASS**
Expected Results and Procedural Comments		
Purpose: To verify that the PSE removes power if the Iport exceeds the specified limits. a. If the DUT supports classification, then the value of I_{CUT} should be between P_class/44 to 400mA, otherwise I_{CUT} is between15.4/Vport and 400mA (inclusive). b. The voltage at the PI of the DUT should be between 44 to 57V (inclusive).		
Comments on Test Results		
a. I_{CUT} = 410 mA b. V_{Port} (min) = 48.9 V		

Test # and Label	Part(s)	Result(s)
33.3.2 – Overload Time Limits	**a**	**PASS**
Expected Results and Procedural Comments		
Purpose: To verify that the PSE removes power if the Iport exceeds I_{CUT} for greater than overload time interval. a. The overload time limit (T_{ovld}) should be between 50ms and 75ms (inclusive).		
Comments on Test Results		
a. T_{ovld} = 62 ms		

Test # and Label	Part(s)	Result(s)
33.3.3 – Inrush Current	**a**	**WARNING**
	b	**Not Available**
Expected Results and Procedural Comments		
Purpose To verify that the PSE will start removing power from the PI within T_{LIM} when it detects a short circuit condition. a. The inrush current at the PI of the DUT should be between 400 to 450mA (inclusive). b. The inrush current at the PI of the DUT should be at least 60mA.		
Comments on Test Results		
a. The inrush current measured after 1ms was 655mA, however this only lasted for another 2ms before dropping to a level current draw of 410mA. b. This test is currently under development.		

Test # and Label	Part(s)	Result(s)
33.3.4 – Short Circuit Time Limit	**a**	**PASS**

Expected Results and Procedural Comments

Purpose To verify that when the PSE detects a short circuit condition it starts removing power from the PI within T_{LIM} and must be done removing power within the conformant time limit.

a. The short circuit time limit (T_{LIM}) should be between 50ms and 75ms (inclusive).

Comments on Test Results

a. T_{LIM} = 62 ms

Test # and Label	Part(s)	Result(s)
33.3.5 – Error Delay Timing	**a**	**PASS**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the PSE waits for at least the minimum conformant time before attempting subsequent detection after it removes power due to detection of error condition.

a. The DUT should wait for at least 750ms after detecting a short circuit condition and removing power before resuming detection
b. The DUT should wait for at least 750ms after detecting an overload condition and removing power before resuming detection

Comments on Test Results

a. The DUT was observed to wait 2.0 s after a short circuit event before resuming signature detection.
b. The DUT was observed to wait 2.0 s after an overload event before resuming signature detection.

Test # and Label	Part(s)	Result(s)
33.3.6 – Range of T_{MPDO} Timer	**a**	**PASS**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that PSE correctly monitors the PD Maintain Power Signature

a. *DC disconnect:* 300ms $\leq T_{MPDO} \leq$ 400ms
b. *AC disconnect:* 300ms $\leq T_{MPDO} \leq$ 400ms

Comments on Test Results

a. *DC disconnect:* 348 ms $\leq T_{MPDO} \leq$ 351 ms
b. The DUT does not monitor ACMPS components.

Test # and Label	Part(s)	Result(s)
33.3.7 - PD MPS Dropout Current Limits (I_{MIN} measurement)	**a**	**PASS**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that PSE correctly monitors the PD Maintain Power Signature for DC disconnect.

a. The DUT may remove power if the current drawn is between 5 mA and 10 mA ($I_{MIN2\ (max)}$) for 400 ms.
b. The DUT must remove power if the current drawn is less than 5 mA ($I_{MIN1\ (max)}$) for 400 ms.

Comments on Test Results

a. 5.0 mA ≤ $I_{MIN2\ (max)}$ ≤ 5.1 mA
b. The DUT removes power when current draw is less than 5mA.

Test # and Label	Part(s)	Result(s)
33.3.8 – PD MPS Time for Validity	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the PSE waits for at least the minimum MPS validity time when it monitors the DC MPS component.

a. The DUT should not remove power from a PD that provides a valid DC MPS signature for at least T_{MPS} every T_{MPS}+T_{MPDO}.

Comments on Test Results

a. The DUT was observed to remain powering when a valid DC MPS signature was presented for at least T_{MPS} every T_{MPS}+T_{MPDO}.

Test # and Label	Part(s)	Result(s)
33.3.9 – AC MPS Signal Parameters	**a**	**Not Applicable**
	b	**Not Applicable**
	c	**Not Applicable**

Expected Results and Procedural Comments

Purpose: To verify that the PI probing AC signals fall within the conformance limits.

a. The PI probing AC voltage (V_open) should be between 1.9V to 10% of Vport (V_{pp}).
b. The AC probing signal frequency should not be greater than 500 Hz.
c. The AC probing signal slew rate should not be greater than 0.1V/µs.

Comments on Test Results

The DUT does not monitor ACMPS components.

Test # and Label	Part(s)	Result(s)
33.3.10 – AC Disconnect Detection Voltages	**a**	**Not Applicable**
	b	**Not Applicable**
Expected Results and Procedural Comments		
Purpose: To verify that the PI probing AC voltages during AC disconnect detection fall within the conformance limits. a. The AC ripple voltage (V_{CLOSE}) should be less than 0.5Vpp. b. The measured V_{Port} (Vp) should not exceed 60V.		
Comments on Test Results		
The DUT does not monitor ACMPS components.		

Test # and Label	Part(s)	Result(s)
33.3.11 – AC MPS Signature	**a**	**Not Applicable**
	b	**Not Applicable**
Expected Results and Procedural Comments		
Purpose: To verify that the PSE that implements AC MPS component correctly monitors the PD Maintain Power Signature. a. The DUT should supply power to the PD for signature impedance less than 27KΩ. b. The measured impedance should be between 27KΩ and 1980KΩ (inclusive).		
Comments on Test Results		
The DUT does not monitor ACMPS components.		

Test # and Label	Part(s)	Result(s)
33.3.12 – Turn Off Time Limits	**a**	**PASS**
Expected Results and Procedural Comments		
Purpose: To verify that the PSE disconnects power within T_{Off} through a test resistor. a. The DUT should remove power in times less than 500ms through a test resistor of 320kΩ.		
Comments on Test Results		
a. The DUT was observed to remove power in less than 1 ms.		

GROUP 4: PSE TRANSMITTER AND RECEIVER CHARACTERISTICS

Test # and Label	Part(s)	Result(s)
33.4.1 – Midspan PSE Return Loss	**a**	**FAIL**

Expected Results and Procedural Comments

Purpose: To verify that the return loss of a Midspan PSE is greater than the minimum conformant value.

a. The DUT's return loss should be greater than 23dB from 1 to 20MHz and greater than 14dB from 20MHz to 100MHz.

Comments on Test Results

Return Loss Margin		
TX pair	(-6.09)	dB
RX pair	(-3.62)	dB

Please refer to the figures appended to the report.

Test # and Label	Part(s)	Result(s)
33.4.2 – Midspan PSE Insertion Loss	**a**	**FAIL**

Expected Results and Procedural Comments

Purpose: To verify that the insertion loss of a Midspan PSE is no greater than the maximum conformant value.

a. The DUT's insertion loss should be no greater than the limit described by equation 33-6 and the maximum conformant value of 0.1dB.

Comments on Test Results

Insertion Loss Margin		
TX pair	(-4.10)	dB
RX pair	(-2.60)	dB

Please refer to the figures appended to the report.

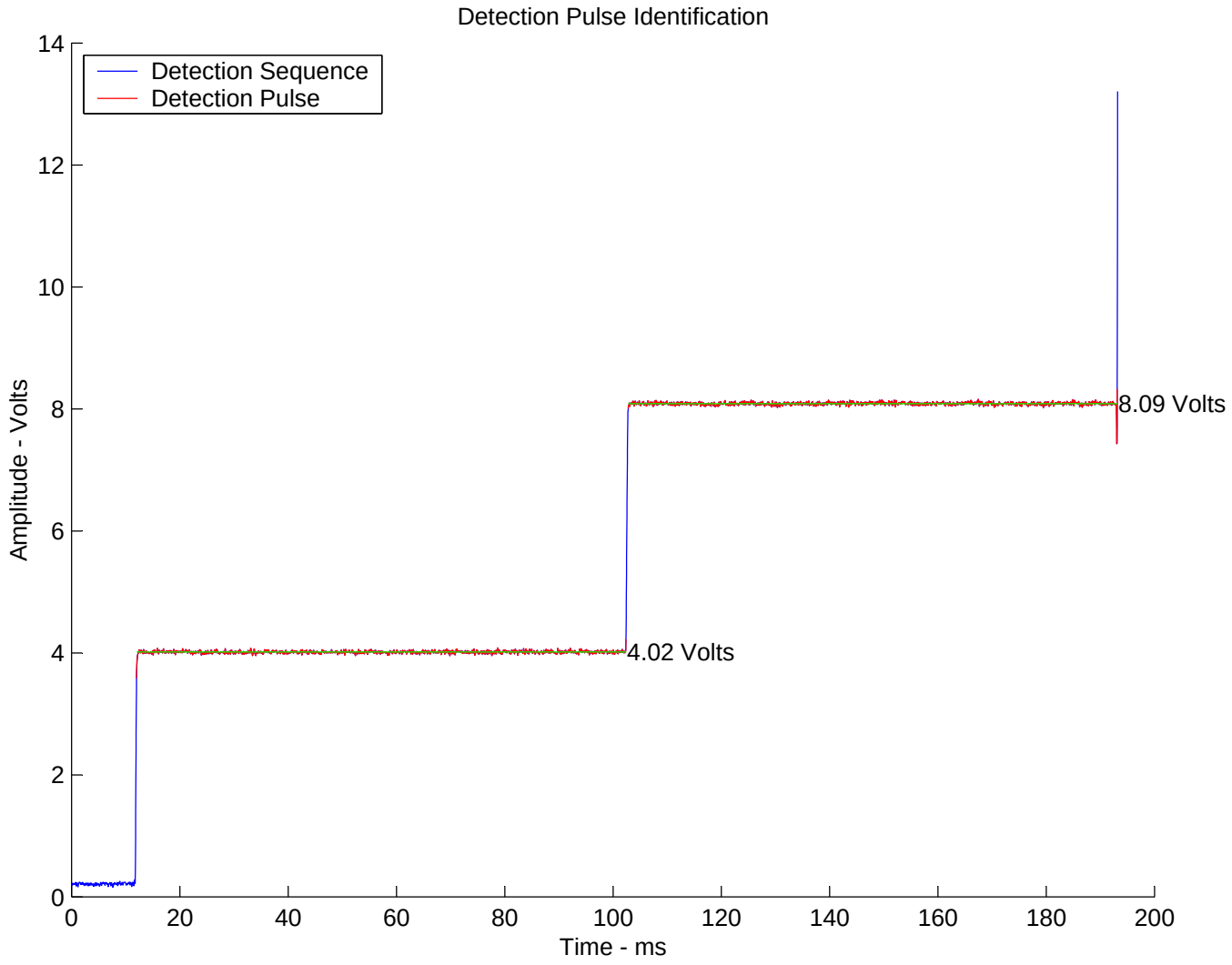
Test # and Label	Part(s)	Result(s)
33.4.3 – Midspan PSE NEXT Loss	**a**	**Not Available**
Expected Results and Procedural Comments		
Purpose: To verify that the NEXT between the transmit and receive pairs of the DUT is within conformance limits. a. The DUT's NEXT loss should be no greater than the limit described by equation 33-5 and the minimum conformant value of 65 dB.		
Comments on Test Results		
This test is currently under development.		

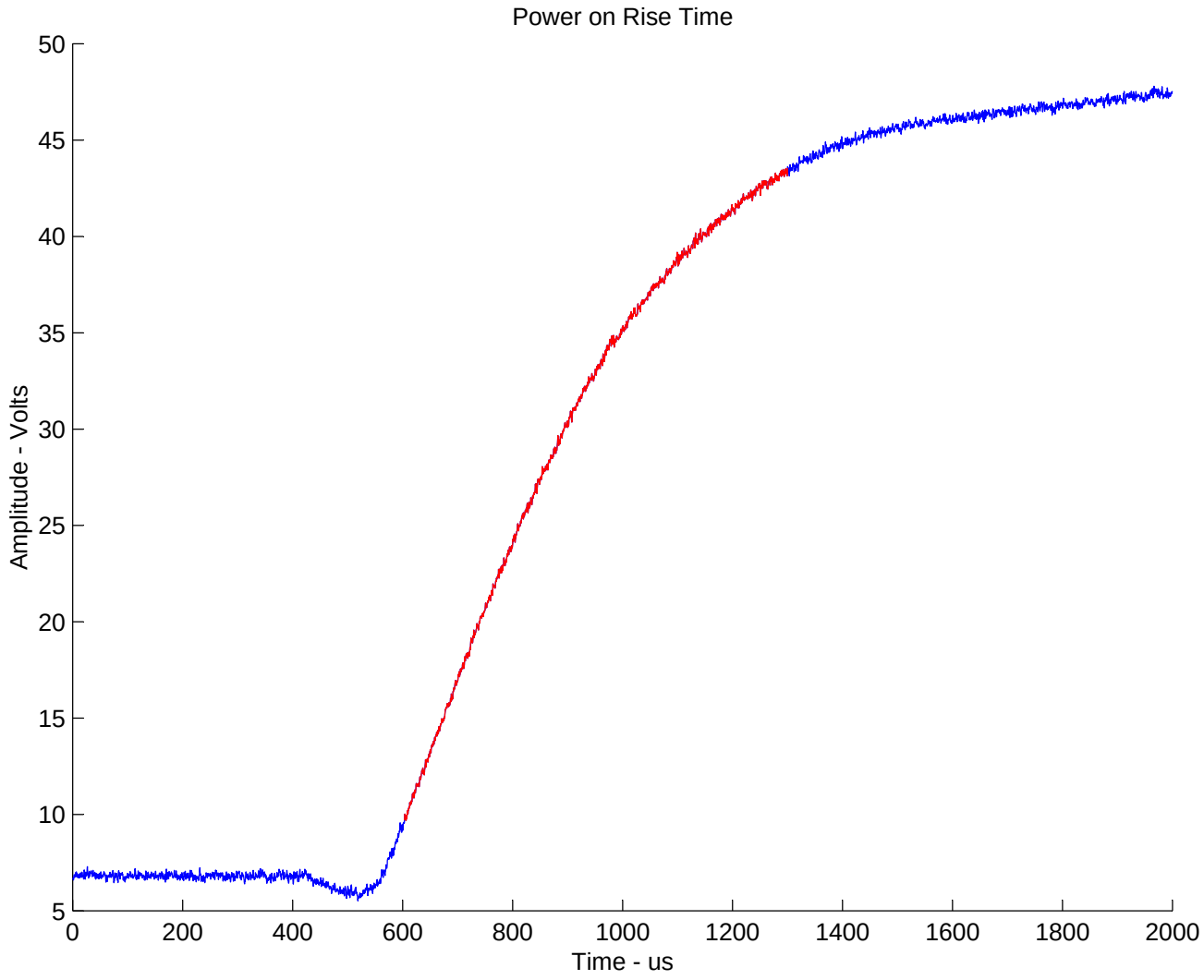
Test # and Label	Part(s)	Result(s)
33.4.4 – PSE Impedance Balance	**a**	**Not Available**
Expected Results and Procedural Comments		
Purpose: To verify that the common-mode to differential-mode impedance balance of the transmit and receive pairs of the PI is greater than the specified limits. a. The common-mode to differential-mode impedance balance for a 100Mb/s transmitter and receiver shall exceed 34-19.2$\log_{10}$(f/50) dB (where f is the frequency in MHz) over the frequency range of 1.0 MHz to 100 MHz		
Comments on Test Results		
This test is currently under development.		

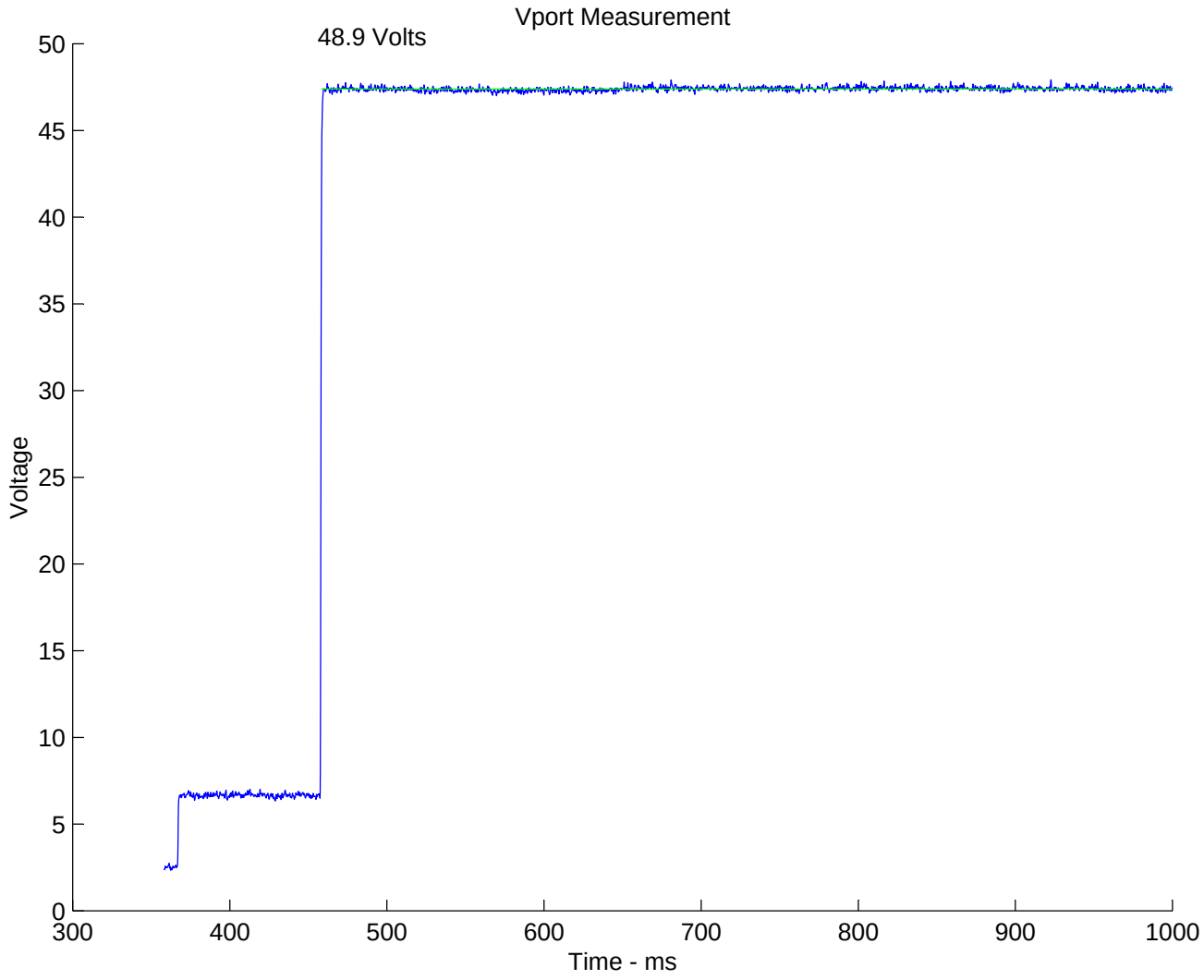
Test # and Label	Part(s)	Result(s)
33.4.5 – PSE Common Mode Output Voltage	**a**	**Not Available**
Expected Results and Procedural Comments		
Purpose: To verify that the common mode AC output voltage at the PI is below the conformant limits. a. The magnitude of the common-mode AC output voltage, *E*cm_out, shall not exceed 50 mV peak when operating at 10 Mb/s, and 50 mV peak-to-peak when operating at 100 Mb/s or greater.		
Comments on Test Results		
This test is currently under development.		

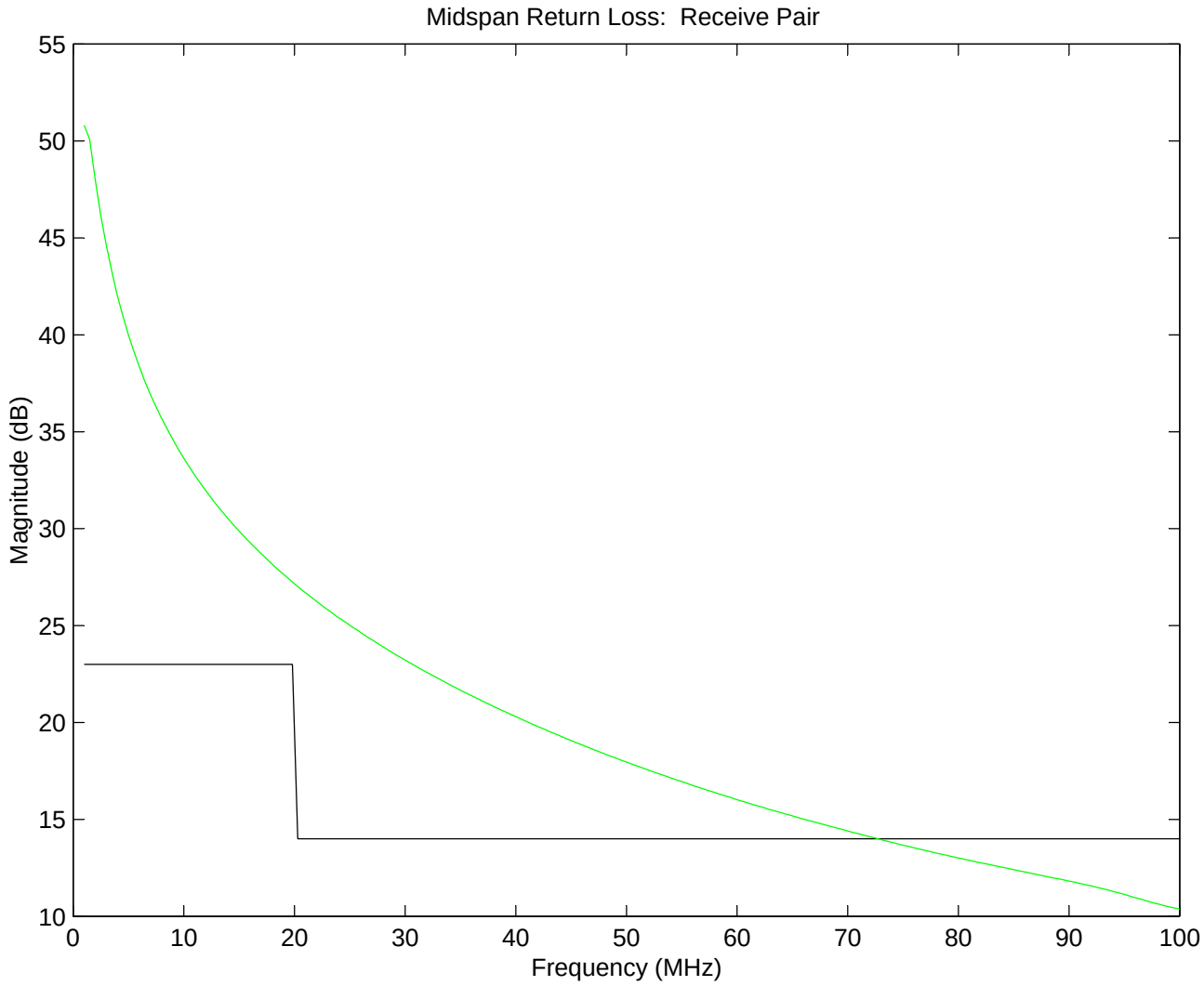
Annex A: Figures

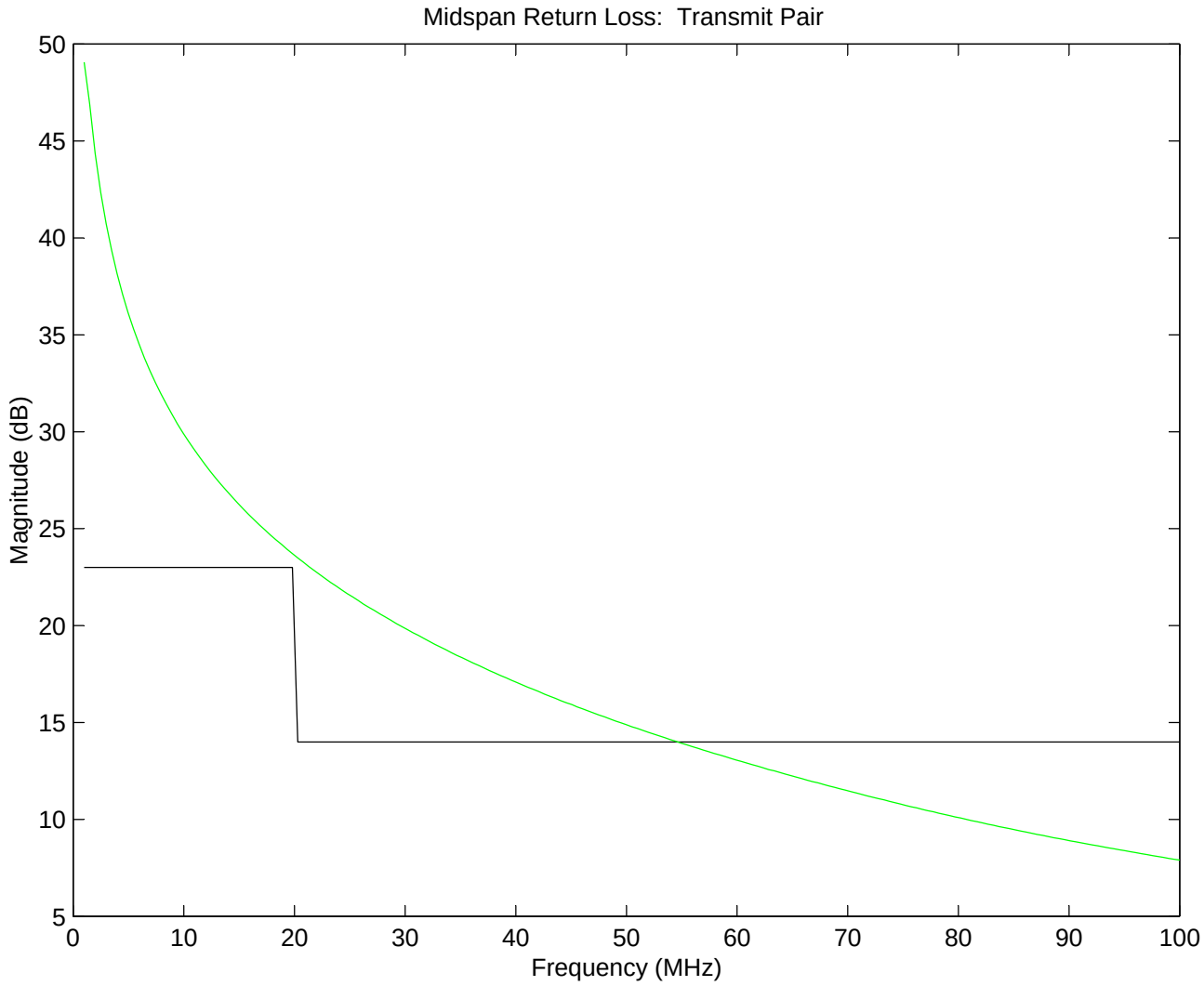
Attached are the figures illustrating the Detection Pulse Sequence, Turn on Rise Time, $V_{PORT,}$ Midspan PSE Return Loss and Midspan PSE Insertion Loss. These were captured either with the real time DSO or the Vector Network Analyzer and post processed using custom Matlab scripts.

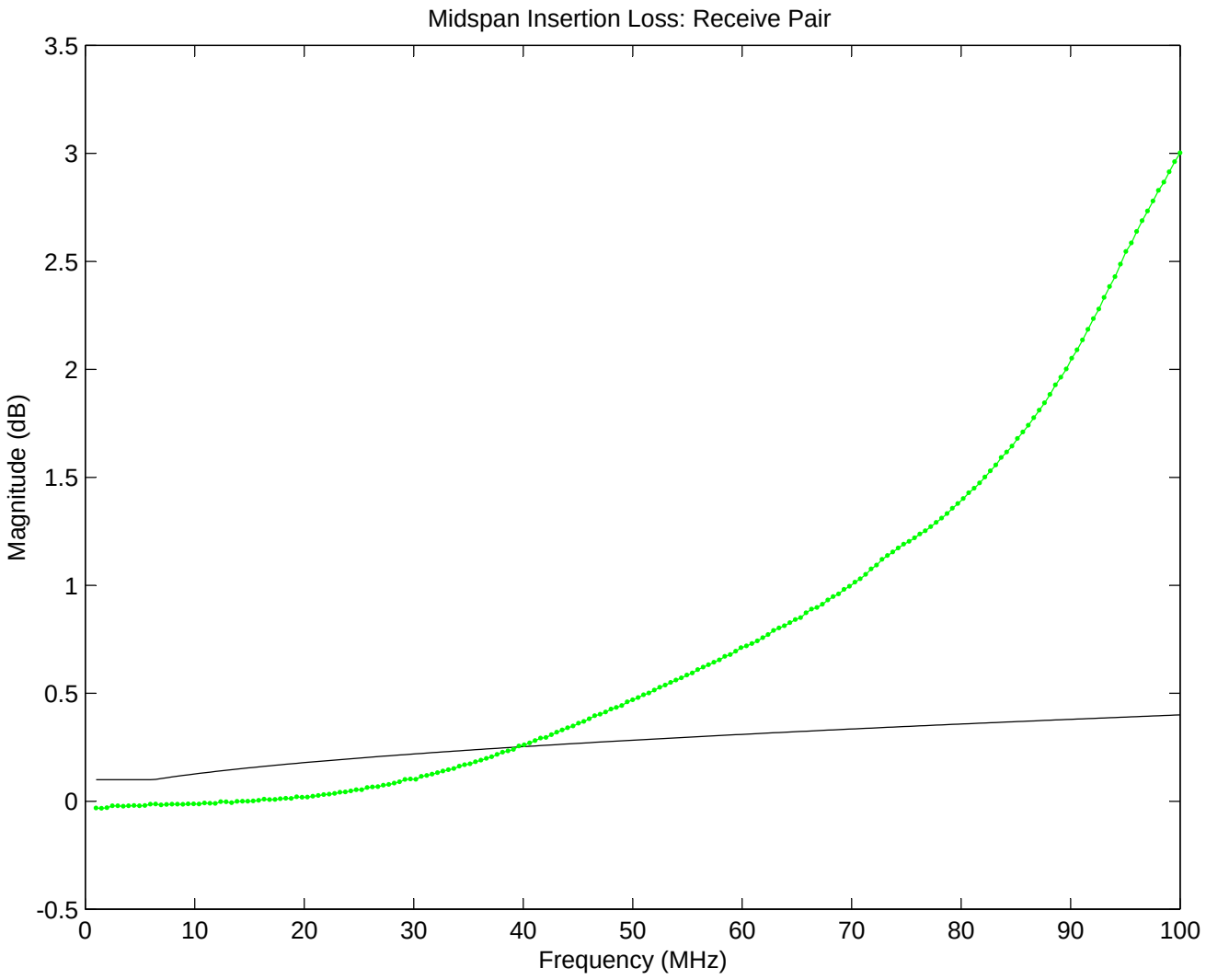

Detection Pulse Identification
Detection Sequence
Detection Pulse
Amplitude - Volts
Time - ms
4.02 Volts
8.09 Volts
0
2
4
6
8
10
12
14
0
20
40
60
80
100
120
140
160
180
200

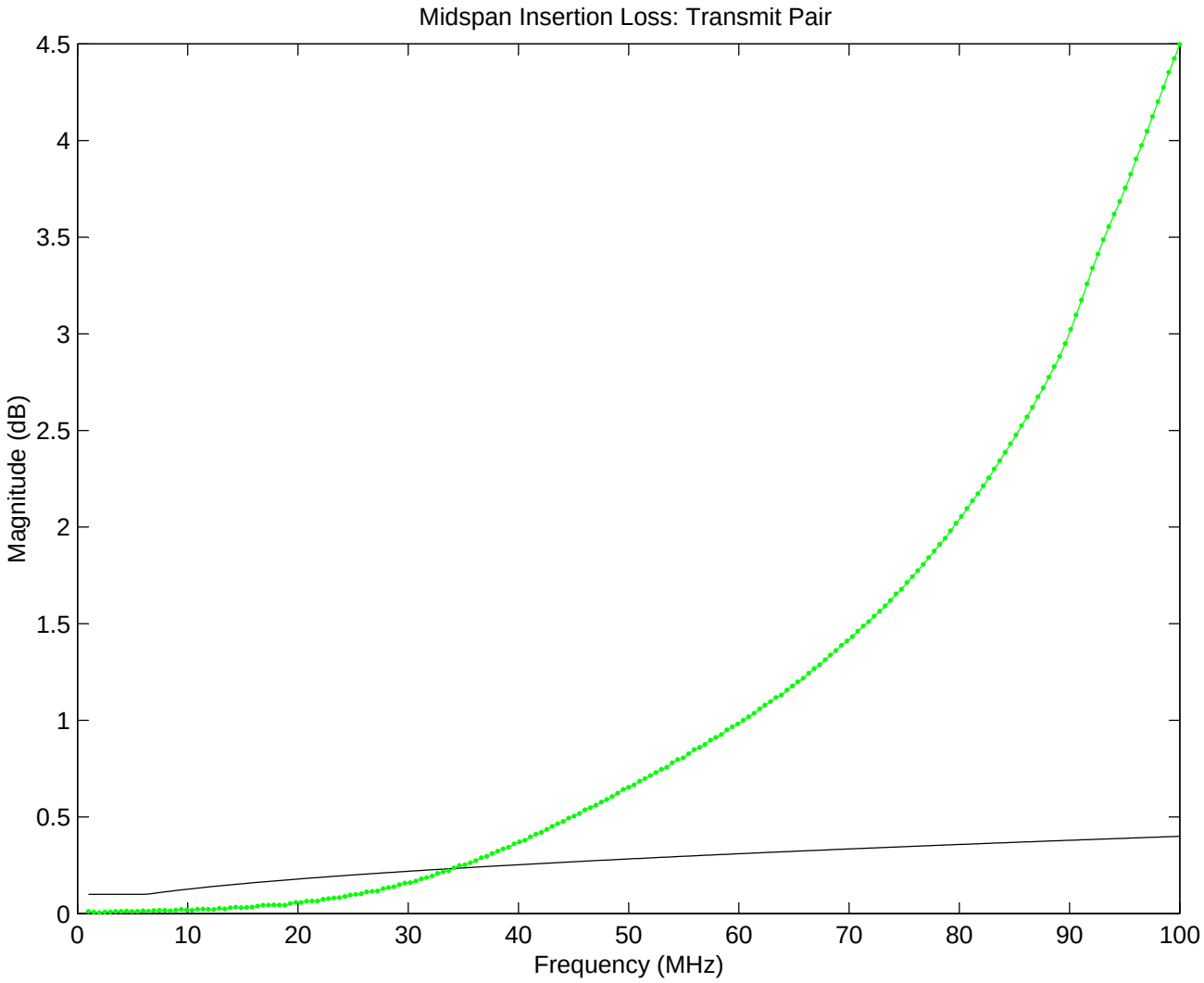

Power on Rise Time
Amplitude - Volts
Time - us
50
45
40
35
30
25
20
15
10
5
0
200
400
600
800
1000
1200
1400
1600
1800
2000


Vport Measurement
48.9 Volts
Voltage
Time - ms
0
5
10
15
20
25
30
35
40
45
50
300
400
500
600
700
800
900
1000


Midspan Return Loss: Receive Pair
Magnitude (dB)
55
50
45
40
35
30
25
20
15
10
0
10
20
30
40
50
60
70
80
90
100
Frequency (MHz)


Midspan Return Loss: Transmit Pair
Magnitude (dB)
Frequency (MHz)
50
45
40
35
30
25
20
15
10
5
0
10
20
30
40
50
60
70
80
90
100


Midspan Insertion Loss: Receive Pair
Magnitude (dB)
Frequency (MHz)
3.5
3
2.5
2
1.5
1
0.5
0
-0.5
0
10
20
30
40
50
60
70
80
90
100


Midspan Insertion Loss: Transmit Pair
Magnitude (dB)
Frequency (MHz)
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
0
10
20
30
40
50
60
70
80
90
100